AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1 and 12 as shown below.

Please **ADD** claims 29-40 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A thin film transistor array substrate for a liquid crystal display, comprising:

a substrate;

a gate line assembly formed on the substrate and transferring gate signals, the gate line assembly comprising gate lines extending in a row direction, and gate electrodes connected to the gate lines;

a storage capacitor line assembly extending in the row direction;

a gate insulating layer formed on the substrate and covering the gate lines and the storage capacitor line assembly;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a data line assembly formed on the gate insulating layer, the data line assembly comprising:

data lines crossing over the gate lines, the data lines and the gate lines define pixel regions;

source electrodes formed on the semiconductor pattern and connected to the data lines; and

drain electrodes formed on the semiconductor pattern and facing the source electrodes around the gate electrodes;

a protective layer covering the data line assembly and the semiconductor pattern, the protective layer having first and second contact holes and being in direct contact with an upper surface of the semiconductor pattern between the source electrode and the drain electrode;

pixel electrodes formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the first contact holes; and

repair members provided corresponding to the pixel regions,

wherein each repair member is extended from the pixel electrode ~~of the~~ corresponding thereto ~~pixel region~~ and overlaps a gate line of an adjoining pixel region on a previous row ~~rows~~.

2. (Previously Presented) The thin film transistor array substrate of claim 1, further comprising storage capacitor conductive patterns formed on the gate insulating layer and overlapping the storage capacitor line assembly, the storage capacitor conductive patterns connected to the pixel electrodes through the second contact holes.

3. (Previously Presented) The thin film transistor array substrate of claim 1, wherein the parts of the gate lines overlapping the repair members are narrower than other parts.

4. (Previously Presented) The thin film transistor array substrate of claim 1, further comprising subsidiary repair members disposed between the repair members and the gate lines.

5. (Original) The thin film transistor array substrate of claim 4, wherein the subsidiary repair members are placed on the same plane as the data line assembly.

6. (Previously Presented) The thin film transistor array substrate of claim 1, wherein the storage capacitor line assembly comprises:

double storage capacitor electrode lines horizontally formed at the top and the bottom of each pixel region; and

storage capacitor electrodes vertically formed at the periphery of the pixel region while interconnecting the storage capacitor electrode lines.

7. (Original) The thin film transistor array substrate of claim 1, wherein the repair member is formed with a ring shape.

8-9. (Cancelled)

10. (Previously Presented) The thin film transistor array substrate of claim 1, wherein a size of an overlapped area between the repair member and the gate line of a previous row is ranged from 5 μm^2 to 1000 μm^2.

11. (Previously Presented) The thin film transistor array substrate of claim 1, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source electrodes and the drain electrodes.

12. (Currently Amended) A liquid crystal display, comprising:

a substrate;

a plurality of gate lines extending in a row direction;

a semiconductor pattern covering the gate lines;

a plurality of data lines extending in a column direction, wherein the data lines and the gate lines define pixel regions;

a plurality of source electrodes formed on the semiconductor pattern;

a plurality of drain electrodes formed on the semiconductor pattern;

a plurality of pixel electrodes formed in the respective pixel regions;

a protective layer covering the data lines and being in direct contact with an upper surface of the semiconductor pattern between the source electrode and the drain electrode;

a plurality of storage capacitance lines overlapped with the respective pixel regions; and

a plurality of extensions provided to the respective pixel regions, ~~wherein~~ each extension being ~~is~~ extended from the pixel electrode corresponding thereto ~~of the respective pixel region~~ and overlapping the gate line ~~of~~ on a previous row.

13. (Previously Presented) The liquid crystal display of claim 12, wherein the storage capacitance lines are extended parallel to the gate lines in the row direction.

14. (Previously Presented) The liquid crystal display of claim 12, wherein the extensions have a ring shape.

15. (Previously Presented) The liquid crystal display of claim 12, wherein a portion of the gate lines overlapped by the extension is narrower than other portions thereof.

16. (Previously Presented) The liquid crystal display of claim 12, further comprising a plurality of conductive patterns formed between the extensions and the gate lines of the previous rows.

17. (Previously Presented) The liquid crystal display of claim 16, wherein the conductive patterns are formed on the same plane as the data lines.

18. (Previously Presented) The liquid crystal display of claim 12, wherein a size of an overlapped area between each extension and the gate line of a previous row is in a range from 5 μm^2 to 1000 μm^2.

19. (Previously Presented) The liquid crystal display of claim 12, further comprising a plurality of storage capacitor conductive patterns overlapping the respective storage capacitance lines, and connected to the respective pixel electrodes.

20. (Previously Presented) A thin film transistor array substrate for a liquid crystal display, comprising:

a substrate;

a gate line assembly formed on the substrate and comprising gate lines extending in a row direction, and gate electrodes connected to the gate lines;

a storage capacitor line assembly extending in the row direction;

a gate insulating layer formed on the substrate and covering the gate lines and the storage capacitor line assembly;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a data line assembly formed on the gate insulating layer, the data line assembly comprising:

data lines crossing over the gate lines, the data lines and the gate lines define pixel regions;

source electrodes formed on the semiconductor pattern and connected to the data lines; and

drain electrodes formed on the semiconductor pattern and facing the source electrodes around the gate electrodes;

a protective layer covering the data line assembly and the semiconductor pattern, the protective layer having first and second contact holes;

pixel electrodes formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the first contact holes; and

repair members provided corresponding to the pixel regions, wherein each repair member is extended from the gate line of the adjoining pixel region on the previous row and overlaps the pixel electrode of the corresponding pixel region.

21. (Previously Presented) The thin film transistor array substrate of claim 20, further comprising storage capacitor conductive patterns formed on the gate insulating layer and overlapping the storage capacitor line assembly, the storage capacitor conductive patterns connected to the pixel electrodes through the second contact holes.

22. (Previously Presented) The thin film transistor array substrate of claim 20, wherein the storage capacitor line assembly comprises:

double storage capacitor electrode lines horizontally formed at the top and the bottom of each pixel region; and

storage capacitor electrodes vertically formed at the periphery of the pixel region while interconnecting the storage capacitor electrode lines.

23. (Previously Presented) The thin film transistor array substrate of claim 20, wherein a size of an overlapped area between the repair member and the pixel electrode of a subsequent row is ranged from 5 μm^2 to 1000 μm^2.

24. (Previously Presented) The thin film transistor array substrate of claim 20, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source electrodes and the drain electrodes.

25. (Previously Presented) A liquid crystal display, comprising:

a substrate;

a plurality of gate lines extending in a row direction;

a plurality of data lines extending in a column direction, wherein the data lines and the gate lines define pixel regions;

a plurality of pixel electrodes formed in the respective pixel regions;

a plurality of storage capacitance lines overlapped with the respective pixel regions; and

a plurality of extensions provided to the respective pixel regions, wherein each extension is extended from the gate line on the previous row and overlapping the pixel electrode of the respective pixel region.

26. (Previously Presented) The liquid crystal display of claim 25, wherein the storage capacitance lines are extended parallel to the gate lines in the row direction.

27. (Previously Presented) The liquid crystal display of claim 25, wherein a size of an overlapped area between each extension and the pixel electrode of a subsequent row is in a range from 5 μm^2 to 1000 μm^2.

28. (Previously Presented) The liquid crystal display of claim 25, further comprising a plurality of storage capacitor conductive patterns overlapping the respective storage capacitance lines, and connected to the respective pixel electrodes.

29. (New) The thin film transistor array substrate of claim 1, wherein the gate line assembly further comprises gate pads, and the data line assembly further comprises data pads.

30. (New) The thin film transistor array substrate of claim 29, further comprising subsidiary gate pads formed on the gate pads and subsidiary data pads formed the data pads.

31. (New) The thin film transistor array substrate of claim 30, wherein the subsidiary gate pads, the subsidiary data pads and the pixel electrodes are derived from the same layer.

32. (New) The liquid crystal display of claim 12, further comprising:

a plurality of gate pads connected to the plurality of gate lines, respectively; and

a plurality of data pads connected to the plurality of data lines.

33. (New) The liquid crystal display of claim 32, further comprising:

a plurality of subsidiary gate pads formed on the plurality of gate pads; and

a plurality of subsidiary data pads formed on the plurality of data pads.

34. (New) The liquid crystal display of claim 33, wherein the plurality of subsidiary gate pads, the plurality of subsidiary data pads and the plurality of pixel electrodes are derived from the same layer.

35. (New) The thin film transistor array substrate of claim 20, wherein the gate line assembly further comprises gate pads, and the data line assembly further comprises data pads.

36. (New) The thin film transistor array substrate of claim 35, further comprising subsidiary gate pads formed on the gate pads and subsidiary data pads formed the data pads.

37. (New) The thin film transistor array substrate of claim 36, wherein the subsidiary gate pads, the subsidiary data pads and the pixel electrodes are derived from the same layer.

38. (New) The liquid crystal display of claim 25, further comprising:

a plurality of gate pads connected to the plurality of gate lines, respectively; and

a plurality of data pads connected to the plurality of data lines.

39. (New) The liquid crystal display of claim 38, further comprising:

a plurality of subsidiary gate pads formed on the plurality of gate pads; and

a plurality of subsidiary data pads formed on the plurality of data pads.

40. (New) The liquid crystal display of claim 39, wherein the plurality of subsidiary gate pads, the plurality of subsidiary data pads and the plurality of pixel electrodes are derived from the same layer.